ICECS 2026

Tutorials

Sunday, November 8th

Room: A (the rooms A and B will be defined later)

Tutorial 1 10:00 - 13:00

Title: ***Theory and Applications of Locally-Active Memristors on the Edge of Chaos***

Instructors: **Alon Ascoli[1], Ahmet S. Demirkol[2]**
[1] Department of Electronics and Telecommunications, Politecnico di Torino, Turin, Italy
[2] Faculty of Electrical and Computer Engineering, Dresden University of Technology, Dresden, Germany

Abstract — The inevitable end of the *CMOS scaling law*, together with the need to resolve the long standing *von Neumann* bottleneck, which limits the performance of today's computing machines, as well as with the *Edge Computing* market request for low-power artificially-intelligent, technical systems capable to sense process and store data in the blink of an eye within a compact lightweight physical volume to provide solutions to time-critical problems locally, calls for the development of innovative multi-functional devices operating similarly as the fundamental units in biological neuronal networks. In this regard, a wide class of volatile memristive devices, endowed with the peculiar capability to act as *sources of infinitesimal energy* when biased around appropriate operating points, a property which is also referred to as *Local Activity*, and may be found also in potassium and sodium ion channels across neuronal membranes, provide an unmissable opportunity to cover the aforementioned necessities. Most interestingly, controlling their bias conditions, devices of this kind may further operate on the *Edge of Chaos*, a region of the Local Activity regime, where they acquire a high degree of *excitability* and showcase an *optimum in performance*, which may be harnessed to develop energy-efficient multi-functional bioinspired circuits and systems for various *Artificial Intelligence*-based applications in the years to come.

Room: B

Tutorial 2 11:00-13:00

Title: **Hands-on Bluetooth Low Energy System Design Using PSoC 6**

Instructors: **John Vourvoulakis**
Dept. of Computer, Informatics and Telecommunications Engineering, International Hellenic University

Abstract — This tutorial provides a hands-on introduction to Bluetooth Low Energy (BLE) application development using the PSoC6 device. BLE is a low-power wireless technology for embedded and IoT devices, widely used in wearables, wireless sensors and monitoring systems. The tutorial combines core BLE concepts with firmware development, enabling participants to build a complete application for data exchange with a PC. The tutorial has three sections. The first introduces the BLE model with emphasis on GAP (Generic Access Profile) and GATT (Generic Attribute Profile). GAP concepts include Central and Peripheral roles, advertising, scanning, connection, and disconnection. GATT is presented through its Client-Server model and the structure of Services, Characteristics, Descriptors, Properties, and UUIDs. Communication methods such as Read/Write, Notifications, and Indications are explained. The second section focuses on the event-driven architecture of the PSoC6 BLE stack. A callback-based programming model is used to handle BLE events.
Key events across the lifecycle of a BLE connection, i.e. advertising, connection, service discovery, data exchange, and disconnection, are presented. Core APIs and their integration into the main loop are introduced to explain firmware execution flow. The third section is a hands-on exercise where participants develop a BLE peripheral application on a PSoC6 evaluation board. They design a GATT database by defining services, characteristics and configuring their properties. Firmware is built step by step to support advertising, connection, service discovery, and bidirectional data exchange using Notifications, Indications, and Read/Write operations. UART debugging is used to observe system behavior. Upon completion, participants gain practical experience in developing BLE applications for embedded systems.

Participants are expected to:
1. bring a laptop equipped with an integrated Bluetooth Low Energy adapter or an external Bluetooth 5.0 (or later) USB dongle.
2. install a terminal emulator (e.g., PuTTY).
3. install a BLE client application (e.g., Bluetooth LE Explorer).
4. install the PSoC6 development environment. The exact IDE version and any operating system requirements will be communicated before the tutorial.
5. have prior knowledge of the C programming language.

The instructor will provide CY8PROTO evaluation kits for the hands-on laboratory sessions. Since fifteen evaluation boards are available, participation is limited to fifteen attendees.

Sunday, November 8th, 13:15-15:15

Room: A

Tutorial 3

Title: **Open-Source Physical Design Flows for Monolithic and Heterogeneous 3D ICs using OpenROAD**

Instructors: **George Rafael Goudroumanis[1], Maria Pantazi-Kypraiou[1], Alberto Garcia-Ortiz[2]**
[1]ECE Dpt., University of Thessaly, Volos, Greece
[2]ITEM, University of Bremen, Bremen, Germany

Abstract — This tutorial presents a practical introduction to open-source physical design methodologies for monolithic and heterogeneous three-dimensional integrated circuits (3D ICs) using the OpenROAD framework. As conventional CMOS scaling approaches its limits, 3D integration has emerged as a promising solution for improving performance, energy efficiency, and integration density. Despite growing industrial interest, most publicly available physical design tools remain limited to conventional two dimensional implementations, creating a significant barrier for researchers, educators, and practitioners interested in exploring 3D integration technologies.

The tutorial demonstrates how an existing two-dimensional (2D) OpenROAD implementation flow can be systematically extended to support both monolithic and heterogeneous multitier integrated circuits without requiring modifications to Open-ROAD's optimization engine. Participants will learn how technology libraries, placement rows, routing resources, and design exchange formats such as LEF, DEF, and Liberty can be adapted to represent multi-tier designs while maintaining compatibility with established physical design workflows.

The session follows a complete design example that progressively evolves from a conventional synthesized RISC-V implementation into both monolithic and heterogeneous 3D realizations. Each stage of the implementation flow, including floorplanning, placement, clock-tree synthesis, power delivery network generation, routing, and physical verification, is discussed together with the practical considerations introduced by multi-tier integration. Live demonstrations and guided examples, which will be made publicly available, illustrate how automation scripts and open-source infrastructure enable reproducible research without relying on proprietary design tools or commercial process design kits (PDKs).

By combining theoretical foundations with hands-on implementation techniques, the tutorial equips participants with the knowledge required to develop, reproduce, and extend open-source 3D physical design flows. It also discusses current research challenges, including technology-aware placement, automated partitioning, cross-tier optimization, and heterogeneous integration, providing attendees with a foundation for future research and practical development in emerging semiconductor technologies.

Room: B

Tutorial 4

Title: **Cross-Layer Co-Design of FeFET-Based Compute-in-Memory Architectures: From Device Physics to full Accelerator Design**

Instructors: **Thomas Kämpfe[1], Nellie Laleni[2], Alptekin Vardar[3]**
[1] Fraunhofer IPMS Dresden and TUB Braunschweig.
[2] Fraunhofer IPMS Dresden and ETH Zurich.
[3] Fraunhofer IPMS Dresden and TUM Munich.

Abstract — The rapid growth of artificial intelligence (AI) has significantly increased the demand for hardware platforms capable of delivering high computational performance while maintaining low energy consumption. Conventional von Neumann architectures are increasingly constrained by the memory bottleneck, motivating the development of Compute-in-Memory (CIM) techniques that perform computation directly within memory arrays. Among the emerging memory technologies, ferroelectric field-effect transistors (FeFETs) have attracted considerable interest due to their nonvolatile operation, CMOS compatibility, scalability, and suitability for analog and mixed-signal in-memory computing. This tutorial presents a comprehensive overview of the cross-layer co-design methodology required to develop FeFET-based Compute-in-Memory architectures, bridging the gap between device physics and circuit and system design. It introduces AI hardware acceleration, CIM fundamentals, analog, digital and mixed-signal paradigms, and compares different non-volatile-memory (NVM) technologies.
Building upon these foundations, the tutorial explores FeFET device operation, programming characteristics, variability, endurance, retention, and both binary and multi-level-cell (MLC) configurations. FeFET memory cells, array organizations, and analog computation mechanisms are discussed together with current-domain and charge-domain computing, sensing techniques, analog front-end circuits, and ADC architectures. In addition, the tutorial covers digital Compute-in-Memory architectures, peripheral digital circuits, hardware integration, and system-level design considerations, providing attendees with a comprehensive overview of modern FeFET-based CIM systems. The tutorial demonstrates how device, circuit, architecture and algorithmic considerations are jointly optimized through a cross-layer co-design approach. Representative simulation and experimental results illustrate practical methodologies, design trade-offs and current research challenges. The tutorial targets graduate students, researchers and engineers working in integrated circuits, semiconductor devices and Compute-in-Memory design.

Sunday, November 8th, 15:30-17:30

Room: A

Tutorial 5

Title: **Physical Attacks: Power Analysis against Cryptographic Devices**

Instructors: **Martin Schmid[1,2], Prof. Dr.-Ing. Elif Bilge Kavun[2]**
University of Passau[1], Dresden University of Technology[2], Germany

Abstract — Cryptographic implementations in digital circuits are prone to side-channel analysis attacks, where an attacker extracts the secret by monitoring physical characteristics of the implementation that lie outside its logical response behavior. Most prominently, a circuit's instantaneous power consumption can leak the secret in practice, even while the underlying cryptographic algorithm is mathematically secure. This gap between algorithmic and implementation security is easy to overlook, and designers of digital systems must be aware of it.
Power analysis is widely regarded as the most powerful of these attacks. For many implementations, it can be carried out with low-cost equipment and requires only modest knowledge of the internal structure of the target device. In this tutorial, you will learn the fundamentals of physical attacks, with a focus on power analysis. We will first examine why CMOS circuits leak, then study how a device's power consumption is captured and how the resulting traces are exploited to recover a secret key using differential power analysis. The lecture concludes with a case study from our own research showing how these attacks extend to targets beyond the textbook setting, and an overview of countermeasures, including hiding and masking.
In a concluding hands-on exercise, you will implement a differential power analysis attack within a guided notebook, recovering the secret key of an AES implementation from real, prerecorded power traces. By the end, you will understand how power leakage arises in hardware and will have gained practical experience in recovering a key through differential power analysis. No prior background in cryptography or side-channel analysis is required. Basic knowledge of Python is useful to participate in the hands-on exercises. The exercise notebook will be hosted online; therefore, a tablet/laptop with a browser suffices.

Materials provided: Slide deck, Google Colab notebook with pre-captured power traces.
Equipment: Projector. Participants better to bring their tablet/laptop to solve the exercises.

Practical part
The exercise asks the participants to implement a working DPA attack. The Colab notebook provides a Python code skeleton (which supplies trace loading, the intermediate-value/S-box helper, and plotting utilities), real pre-recorded power traces, a description of the AES core on which they were captured, and introductory instructions. The participants implement the difference-of-means analysis themselves, grouping the traces by an intermediate-value hypothesis and ranking the key candidates. If successful, they recover the secret key.

Room: B

Tutorial 6

Title: **Architecting Low-Power Frequency Generation Units in FD-SOI: single- and Multi-Loops for IoT, ISAC, and Automotive**

Instructors: **Yann Deval,**
University of Bordeaux / IMS Laboratory, France

Abstract — Low-power frequency generation units (FGUs) are becoming decisive blocks in RF system-on-chips for battery-powered IoT, automotive sensing, integrated sensing and communication (ISAC), space/harsh-environment radios, and always-on edge-AI nodes. These applications impose contradictory requirements: microwatt-to-milliwatt power budgets, low integrated jitter and close-in phase noise, agile channel hopping, fast start-up or wake-up, and robust operation across process, voltage, temperature, aging, and radiation stress. This tutorial presents a circuit-to-system view of modern phase-locked loops that addresses these trade-offs through multi-loop frequency synthesis.

The tutorial begins by translating application specifications into PLL metrics - phase-noise masks, rms jitter, reference spur limits, settling time, energy per lock, and frequency plan constraints. It then compares classical analog PLLs, all-digital PLLs, sub-sampling PLLs, and hybrid architectures, emphasizing dual-loop strategies that separate coarse acquisition from fine low-noise tracking. Design examples show how digital calibration, TDC/DTC linearization, DCO/VCO gain management, loop-bandwidth scheduling, divider-noise mitigation, and spur-aware layout choices interact. Particular attention is given to architectures that can switch operating modes between acquisition, tracking, standby, and recalibration without losing spectral purity.

A dedicated section connects these architectures to FD-SOI and RF-SOI technology opportunities. In line with the European SOIL project, FD-SOI is treated not only as a low-power technology option but as an enabler of reconfigurable RF integrated circuits through efficient body biasing, adaptive oscillators, low-leakage digital control, and single-chip digital, analog, and RF integration. The tutorial concludes with design checklists, figure-of-merit comparisons, reliability/automotive considerations, and open research directions for low-power PLLs in future IoT, automotive radar, 5G/6G connectivity, and ISAC platforms. Attendees will leave with practical trade-off maps and a methodology for selecting, sizing, calibrating, and verifying a PLL architecture against application-level constraints, while understanding how technology choices, architecture partitioning, and measurement strategy jointly determine power, noise, locking speed, robustness, and industrial readiness for emerging European and global applications.